Amendment

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-13. (Canceled).

14. (currently amended): An integrated circuit chip package comprising:

an integrated circuit chip having a plurality of edges and tips and attached to a substrate, wherein each tip is at a position where several edges meet;

a stress buffering material only covering portions ~~corners~~ of said integrated circuit chip which are neighboring the tips; and

an encapsulation material coating said integrated circuit chip and a portion of said substrate.

15. (Original): The package according to claim 14 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

16. (currently amended): The package according to claim 14 wherein said integrated circuit chip is attached to said substrate by a super ball grid array(SBGA) ~~like~~ structure.

17. (currently amended): The package according to claim 14 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at said portions ~~corners~~ of said integrated circuit chip.

18. (Original): The package according to claim 14 wherein said stress buffering material comprises an epoxy or resin.

19. (Original): The package according to claim 14 wherein said stress buffering material has a low coefficient of thermal expansion.

20. (Original): The package according to claim 21 wherein said integrated circuit chip contains low dielectric constant dielectric layers.

21. (currently amended): An integrated circuit chip package comprising:

an integrated circuit chip ~~having a first surface and a second surface opposite thereto, wherein said second surface is~~ having a plurality of edges and tips and attached to a substrate, wherein each tip is at a position where several edges meet;

a stress buffering material having a substantially equal coefficient of thermal expansion to said integrated circuit chip, ~~covering at least one corner of said integrated circuit chip ,wherein a part of the first surface is not covered by the stress buffering material~~ and only covering portions of said integrated circuit chip which are neighboring the tips; and

an encapsulation material covering said integrated circuit chip and said stress buffering material.

22. (currently amended): The package according to claim 21 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at ~~least one corners~~ said portions of said integrated circuit chip.

23. (previously presented): The package according to claim 21 wherein said stress buffering material comprises an epoxy or resin.

24. (previously presented): The package according to claim 21 wherein said stress buffering material has a low coefficient of thermal expansion.

25. (previously presented): The package according to claim 21 wherein said integrated circuit chip contains low dielectric constant dielectric layers.

26. (previously presented): The package according to claim 21 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

27. (currently amended): The package according to claim 21 wherein said integrated circuit chip is attached to said substrate by a super ball grid array (SBGA) ~~like~~ structure.